Seat Number _____ **Tomasulo Coding Form** Name _____

Architecture

Number of Reservation Stations				Number of Units		Latency			
load	store	fadd	fmul	FP add	FP mult	load	fadd	fmul	fdiv
5	5	3	2	1	1	1	2	10	40

Assume that the second instruction is waiting for memory and that all instructions have issued. Then in cycle 10, the second instruction accesses memory. Show the results before cycle 10.

Instruction Summary

Insruction		Reservation Station	Execution Unit	Cycle					Write dest
				Issue	Ex Start	Ex End	Memory	CDB	
L.D	F6,32(R2)	Load1	ALU	1	2	2	3	4	F6
L.D.	F2,44(R3)	Load2	ALU	2	3	3			F2
MUL.D	F0,F2,F4	Mult1	fmul	3					F0
SUB.D	F8,F2,F6	Add1	fadd	4					F8
DIV.D	F10,F0,F6	Mult2	fmul	5					F10
ADD.D	F6,F8,F2	Add2	fadd	6					F6

Reservation Stations

Name	Busy	Op	Vj	Vk	Qj	Qk	A
Load1	No						
Load2	Yes	Load					44 + Regs[R3]
Add1	Yes	SUB		Mem[32+Regs[R2]]	Load2		
Add2	Yes	ADD			Add1	Load2	
Add3	No						
Mult1	Yes	MUL		Regs[F4]	Load2		
Mult2	Yes	DIV		Mem[32+Regs[R2]]	Mult1		

Register Status

F0	F2	F4	F6	F8	F10	F12	F14
Mult1	Load2		Add2	Add1	Mult2		