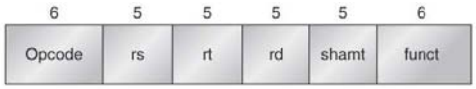
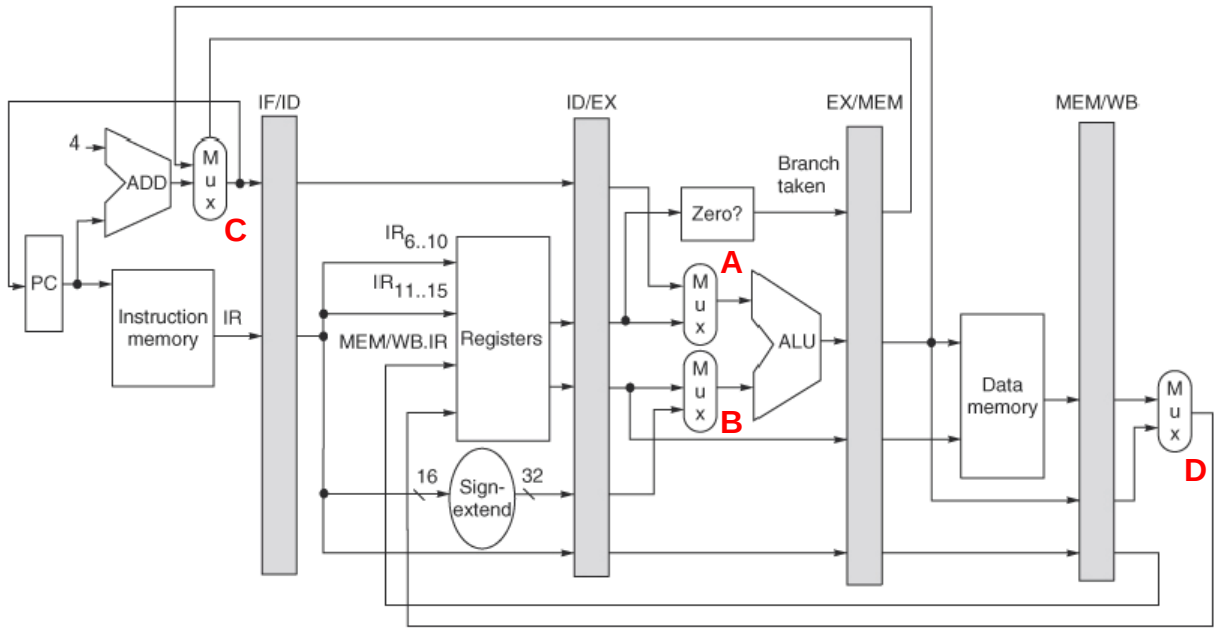
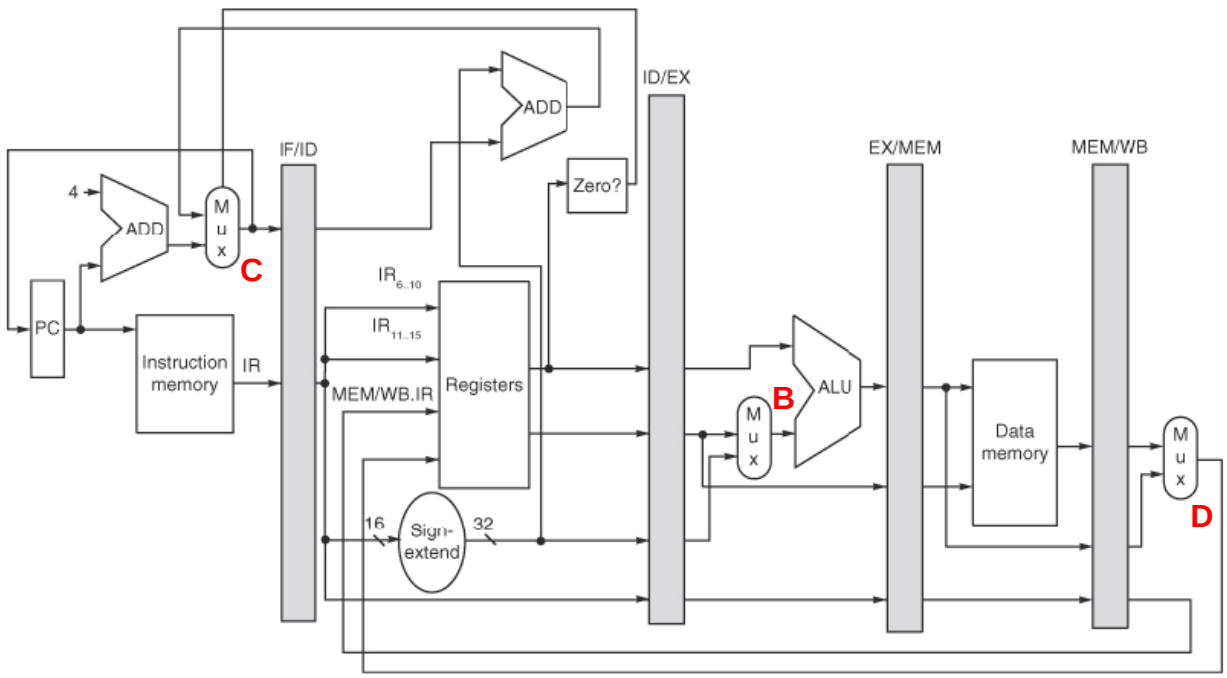
load: Regs[rt] ← Mem[Regs[rs] + Imm]
store: Mem[Regs[rs] + Imm] ← Regs[rt]
branch: if (Regs[rs] == 0) PC ← PC + (Imm << 2)
Immediate ALU: Regs[rt] ← Regs[rs] *op* Imm



RR ALU: Regs[rd] ← Regs[rs] *funct* Regs[rt]



Basic Pipeline



Pipeline that eliminates some branch stalls