CS 3853 Midterm Exam 1 Solutions — Fall 2013

1) (4 points) $\frac{E_B}{E_A} = 1.4$ and $E_B = 8$ so $E_A = 8/1.4 = 5.7143$ seconds.

2) (4 points) $\frac{E_B}{E_A} = 1.4$ and $E_A = 8$ so $E_B = 1.4 \times 8$ = 11.2 seconds.

3) (4 points) $\frac{E_B}{E_A} = 1.4$ and $\frac{E_C}{E_B} = 1.7$ so $\frac{E_C}{E_A} = 1.4 \times 1.7 = 2.55$

4) (4 points) $\frac{E_B}{E_A} = 1.5$ and $\frac{E_C}{E_A} = 1.7$ so $\frac{E_C}{E_B} = 1.7/1.5 = 1.1333$, so B is 13.33% faster than C.

5) (4 points) $\frac{5{,}000{,}000{,}000}{700{,}000{,}000} = x^5$, so $x^5 = 50/7$, so $x = 1.48175$. $x^{12} = 112.019$, so $112.019 \times 5 \times 10^9 = 5.601 \times 10^{11}$.

6) (4 points) If the power supply MTTF is x hours, failure rate = $\frac{7}{1{,}200{,}000} + \frac{2}{x} = \frac{1}{100{,}000}$ so x = 480,000, and the answer is 480,000 hours.

7) (8 points, 4 points each)
   a) $E_B = .8E_B + .2E_B$ and $E_A = .8E_B + .2 \times 1.65E_B = 1.13E_B$ so $\frac{E_A}{E_B} = 1.13$.
   b) $E_A = .8E_A + .2E_A$ and $E_B = .8E_A + .2/1.65E_A = .9212E_A$, so $\frac{E_A}{E_B} = 1/.9212 = 1.0855$

8) (4 points) $E_A = .8E_A + .2E_A$ and $E_B = .8/1.4E_A + .2/1.9E_A = .6767E_A$, so $\frac{E_A}{E_B} = 1/.6767 = 1.4778$

9) (9 points)
   a) The value of R2 and 3 are added and the result is stored in the EX/MEM pipeline register. Also, at least part of the instruction (the destination register address) is copied from ID/EX to EX/MEM. At least 2 control bits are also copied (branch taken and WB?) from ID/EX to EX/MEM.
   b) The value of R2 and 8 are added and the result is stored in the EX/MEM pipeline register. Also, part of the instruction (the destination register address) is copied from ID/EX to EX/MEM. At least 2 control bits are also copied (branch taken and WB?) from ID/EX to EX/MEM.

10) (10 points, 2 point for each part)

		select input			
	Instruction	Mux A	Mux B	Mux C	Mux D
a)	`DADD R1, R2, R3`	1	0	1	1
b)	`DSUB R1, R2, #7`	1	1	1	1
c)	`LD R1, 8(R2)`	1	1	1	0
d)	`SD R1, 8(R2)`	1	1	1	X
e)	`BEQZ R1, loop`	0	1	0	X

11) (10 points, 1 point each)

Description	Value	Description	Value
$IR_{6..10}$	2	$IR_{11..15}$	1
top Registers output	13	bottom Registers output	9
Mux A output	13	Mux B output	3
ALU output	16	Mux D output	16
MEM/WB.IR Register input	1	bottom Registers input	16

13) (3 points)
   a) old = .8 + .2, new = .8/1.4 + .2/s = .57143 + .2/s, where s is the speedup of the floating point processor. Setting 1/(.57143 + .2/s) to 1.5 and solving for s gives 2.1. So we must make the floating point processor 110% faster.
   b) Cannot be done. The maximum speedup is 1.4/.95 = 1.47368.

14) (9 points, 1 point each)

instruction	cycle 30	cycle 31	cycle 32	cycle 33	cycle 34	cycle 35	cycle 36	cycle 37
`DADD R1, R2, R3`	IF	ID	EX	MEM	WB			
`OR R4, R5, R6`		IF	ID	EX	MEM	WB		
`AND R7, R8, #14`			IF	ID	EX	MEM	WB	
`DADD R9, R1, #12`				IF	ID	EX	MEM	WB

Description	cycle	value	Description	cycle	value	Description	cycle	value
$IR_{6..10}$	33	8	$IR_{6..10}$	34	1	$IR_{6..10}$	34	9
Mux B output	33	25	Mux D output	34	36	MEM/WB.IR Registers input	34	1
Mux B output	34	14	Mux D output	37	48	MEM/WB.IR Registers input	35	4

15) (8 points, 1 point each)

a) The first instruction sets R1 in cycle 5 (WB), but the second one needs it in cycle 3 (ID).
b) 2 and 1
c) ID of the second instruction, which is cycle 3
d) ID/EX
e) IF/ID
f) ID of the third instruction, which is cycle 4.
g) EX/MEM
h) IF/ID

12) (15 points, 3 points each)

a) Assume that there is no forwarding.

instruction	cycle 1	cycle 2	cycle 3	cycle 4	cycle 5	cycle 6	cycle 7	cycle 8	cycle9	cycle 10
`DADD R1, R2, R3`	IF	ID	EX	MEM	WB					
`DSUB R4, R5, R6`		IF	ID	EX	MEM	WB				
`AND R7, R8, R9`			IF	ID	EX	MEM	WB			

b) Assume that there is no forwarding.

instruction	cycle 1	cycle 2	cycle 3	cycle 4	cycle 5	cycle 6	cycle 7	cycle 8	cycle9	cycle 10
`DADD R1, R2, R3`	IF	ID	EX	MEM	WB					
`DSUB R4, R5, R1`		IF	stall	stall	ID	EX	MEM	WB		
`AND R7, R8, R9`			stall	stall	IF	ID	EX	MEM	WB	

c) Assume that forwarding is used.

instruction	cycle 1	cycle 2	cycle 3	cycle 4	cycle 5	cycle 6	cycle 7	cycle 8	cycle9	cycle 10
`DADD R1, R2, R3`	IF	ID	EX	MEM	WB					
`DSUB R4, R5, R1`		IF	ID	EX	MEM	WB				
`AND R7, R8, R9`			IF	ID	EX	MEM	WB			

d) Assume that there is no forwarding.

instruction	cycle 1	cycle 2	cycle 3	cycle 4	cycle 5	cycle 6	cycle 7	cycle 8	cycle9	cycle 10
`LD R1, 8(R2)`	IF	ID	EX	MEM	WB					
`DSUB R4, R5, R1`		IF	stall	stall	ID	EX	MEM	WB		
`AND R7, R8, R9`			stall	stall	IF	ID	EX	MEM	WB	

e) Assume that forwarding is used.

instruction	cycle 1	cycle 2	cycle 3	cycle 4	cycle 5	cycle 6	cycle 7	cycle 8	cycle9	cycle 10
`LD R1, 8(R2)`	IF	ID	EX	MEM	WB					
`DSUB R4, R5, R1`		IF	stall	ID	EX	MEM	WB			
`AND R7, R8, R9`			stall	IF	ID	EX	MEM	WB		