Seat Number _____ Name _____

CS 3853 Midterm Exam 1 — Fall 2013

This is a closed book exam. You may use a calculator, as long as it is not capable of accessing a network. No cell phones.
This is a 75-minute exam. The questions are divided into 2 parts. The first part is worth 80 points. Everyone should be able to finish Part 1. Part 2 is worth 20 points. The questions on part 2 are harder. If you cannot do the questions are Part 1 quickly, you may not have time to finish Part 2.
Put your answers in the space provided. You must show your work to get credit. If you cannot fit your answers in the space provided, ask for an additional sheet of paper. You will be given a page of diagrams to refer to for this exam. For this exam, you will not need to refer to the diagram at the bottom of the page. Do not write on the diagrams. You must turn in the diagram sheet with your exam. Do all calculations to at least 4 decimal places.

Part 1: 80 points

1) (4 points) Assume that for a given task, machine A is 40% faster than machine B. If it takes 8 seconds to complete the task on machine B, how long will it take on machine A? **Put a box around your final answer.**

2) (4 points) Assume that for a given task, machine A is 40% faster than machine B. If it takes 8 seconds to complete the task on machine A, how long will it take on machine B? **Put a box around your final answer.**

3) (4 points) Assume that for a given task, machine A is 50% faster than machine B and machine B is 70% faster than machine C. What is the speedup of machine A over machine C? **Put a box around your final answer.**

4) (4 points) Assume that for a given task, machine A is 50% faster than machine B and machine A is 70% faster than machine C. How much faster is machine B than C? **Put a box around your final answer.**

5) (4 points) In 2008 it was possible to put 700,000,000 transistors on a chip and in 2013 it was possible to put 5,000,000,000 transistors on a chip. Assuming the same rate of increase each year, how many transistors would be able to fit on a chip in 2025? **Put a box around your final answer.**

6) (4 points) A system has 7 disk drives, each with a MTTF of 1,200,000 hours, and two identical power supplies. The system will fail if any one component fails. You want the MTTF of the system to be at least 100,000 hours. What is the minimum MTTF for each of the two power supplies? **Put a box around your final answer.**

7) (8 points, 4 points each) Processors A and B are identical, except that processor B executes floating point instructions 65% faster than A. Calculate the speedup if a task spends 20% of its time executing floating point instructions on

a) machine B. **Put a box around your final answer.**

b) machine A. **Put a box around your final answer.**

8) (4 points) A new design makes the floating point processor 90% faster and everything else 40% faster. What is the speedup of a task that originally spent 20% of its time doing floating point operations? **Put a box around your final answer.**

9) (9 points) Describe in words what each of the following instructions does in the EX stage of execution for the hardware shown in the basic pipeline diagram.
   a) **DADD R1, R2, #3**
   b) **LD R1, 8(R2)**

10) (10 points, 2 points each) Consider the Basic Pipeline in the diagram in which the muxes are labeled A, B, C, and D. Suppose a select input of 0 on a mux chooses the upper data input and a select input of 1 chooses the bottom data input. For each of the following instructions, determine the 4 select inputs for the muxes and write your answers in the table below. If the select input does not matter, use an X. Each box must be filled in with 0, 1, or X. For the last instruction, assume that the branch is taken. Be sure to use an X if the select input does not affect the result of the instruction.

		select input			
	Instruction	Mux A	Mux B	Mux C	Mux D
a)	`DADD R1, R2, R3`				
b)	`DSUB R1, R2, #7`				
c)	`LD R1, 8(R2)`				
d)	`SD R1, 8(R2)`				
e)	`BEQZ R1, loop`				

11) (10 points, 1 point each) Refer to the instruction format and the Basic Pipeline in the diagram. Suppose that we are executing the instruction: DADD R1, R2, #3 and that before this instruction executes, R1 = 9, R2 = 13. What are the values on the following lines in the Basic Pipeline diagram? Fill in each table entry with a decimal number.

Description	Value	Description	Value
$IR_{6..10}$		$IR_{11..15}$	
top Registers output		bottom Registers output	
Mux A output		Mux B output	
ALU output		Mux D output	
MEM/WB.IR Register input		bottom Registers input	

12) (15 points, 3 points each) Fill in each of the following timing diagrams for the standard 5-stage pipeline. Assume that the first instruction is fetched in cycle 1.

a) Assume that there is no forwarding.

instruction	cycle 1	cycle 2	cycle 3	cycle 4	cycle 5	cycle 6	cycle 7	cycle 8	cycle 9	cycle 10
`DADD R1, R2, R3`										
`DSUB R4, R5, R6`										
`AND R7, R8, R9`										

b) Assume that there is no forwarding.

instruction	cycle 1	cycle 2	cycle 3	cycle 4	cycle 5	cycle 6	cycle 7	cycle 8	cycle 9	cycle 10
`DADD R1, R2, R3`										
`DSUB R4, R5, R1`										
`AND R7, R8, R9`										

c) Assume that forwarding is used.

instruction	cycle 1	cycle 2	cycle 3	cycle 4	cycle 5	cycle 6	cycle 7	cycle 8	cycle 9	cycle 10
`DADD R1, R2, R3`										
`DSUB R4, R5, R1`										
`AND R7, R8, R9`										

d) Assume that there is no forwarding.

instruction	cycle 1	cycle 2	cycle 3	cycle 4	cycle 5	cycle 6	cycle 7	cycle 8	cycle 9	cycle 10
`LD R1, 8(R2)`										
`DSUB R4, R5, R1`										
`AND R7, R8, R9`										

e) Assume that forwarding is used.

instruction	cycle 1	cycle 2	cycle 3	cycle 4	cycle 5	cycle 6	cycle 7	cycle 8	cycle 9	cycle 10
`LD R1, 8(R2)`										
`DSUB R4, R5, R1`										
`AND R7, R8, R9`										

Part 2: 20 points

13) (3 points) We want to produce a speedup of 1.5. We have already made everything but the floating point operations 40% faster. By what percentage must the floating point processor be improved for a task if for that task the percentage of time it spends on floating point operations with the old design is:
    a) 20%
    b) 5%

    In each case, label you answer and put a box around it.

14) (9 points, 1 point each) This question concerns the Basic Pipeline in the diagram. Consider the sequence of instructions and the initial values of the registers given below.

```
DADD   R1, R2, R3
OR     R4, R5, R6
AND    R7, R8, #14
DADD   R9, R1, #12
```

R1	R2	R3	R4	R5	R6	R7	R8	R9
15	17	19	21	23	25	27	29	31

Assume that the first instruction is fetched in cycle 30. Fill in the following table with the values (in decimal).

Description	cycle	value	Description	cycle	value	Description	cycle	value
$IR_{6..10}$	33		$IR_{6..10}$	34		$IR_{11..15}$	34	
Mux B output	33		Mux D output	34		MEM/WB.IR Registers input	34	
Mux B output	34		Mux D output	37		MEM/WB.IR Registers input	35	

15) (8 points, 1 point each) This problems looks at how the basic pipeline in the figure might handle data hazards. Consider the following two sequences of instructions in which the first instruction of each sequence is fetched in cycle 1:

```
          A)                          B)
DADD R1, R2, R3          DADD R1, R2, R3
AND  R6, R1, R4          OR   R7, R8, R9
                         AND  R6, R1, R4
```

a) Explain why sequence A) has a data hazard when executed by the basic pipeline.
b) How many stall cycles are required to execute each sequence by the basic pipeline? Two answers are required, one of A) and one for B).
c) In which cycle is the stall for sequence A) first detected?
d) To detect the stall for sequence A), the address of the destination register of the first instruction must be compared to the source registers of the second instruction. During the cycle you gave in item c), in which pipeline register is the address of the destination register of the **DADD** instruction stored?
e) During the cycle you gave in item c) for sequence A), in which pipeline register are the addresses of the source register of the **AND** instruction stored?
f) In which cycle is the stall for the sequence B) first detected?
g) For sequence B), during the cycle you gave in item f), in which pipeline register is the address of the destination register of the **DADD** instruction stored?
h) For sequence B), during the cycle you gave in item f), in which pipeline register are the addresses of the source register of the **AND** instruction stored?