Name _____

CS 3853 Computer Architecture Quiz 4b Fall 2013

This is a closed book exam. You may not use a computer, but you may use a calculator.
Answer all question on this sheet in the space required.
Each problem is worth 3 points:

- 1 point for turning in the paper
- 2 points for showing some reasonable work
- 3 points for showing work with the correct answer and if it is numeric, putting a box around the correct answer

1) Explain what is meant by *cache miss penalty*.

2) Assume we have a computer where the CPI is 1 when there are no cache misses. The only data accesses are load and stores and these are 50% of the instructions. The miss penalty is 20 clock cycles and the miss rate is 3%. How much faster would the machine be if all instructions were cache hits?

3) A computer uses 38-bit addresses and a 128K cache which is 2-way set-associative and has a block size of 32. Draw a diagram showing the layout of a memory address. Show the block address, the tag, then index and the block offset, giving the number of bits in each.